26. The system as claimed in claim 25, wherein the processor comprises a first logical processor to execute the first instructions and a second logical processor to execute the second instructions.

27. The system as claimed in claim 25, further comprising a second memory, wherein the first instructions in response to being executed result in the processor initializing the second memory.

28. The system as claimed in claim 25, further comprising an error correction code memory, wherein the second instructions in response to being executed result in the processor initializing the error correction code memory.

29. The system as claimed in claim 25, further comprising a peripheral bus and associated devices, wherein the first instructions in response to being executed result in the processor initializing the peripheral bus and associated devices.

30. The system as claimed in claim 25, further comprising a peripheral component interconnect bus and associated devices, wherein the first instructions in response to being executed result in the processor initializing the peripheral component interconnect bus and associated devices.

31. A method, comprising:

executing with a processor a first startup initialization task; and

executing with the processor at least a portion of a second startup initialization task concurrently with execution of the first startup initialization task.

32. The method as claimed in claim 31, wherein

executing the first startup initialization task comprises a first logical processor of the processor executing the first startup initialization task, and

executing the second startup initialization task comprises a second logical processor of the processor executing the second startup initialization task.

33. The method as claimed in claim 31, wherein executing the second startup initialization task comprises initializing a memory.

34. The method as claimed in claim 31, wherein executing the first startup initialization task comprises initializing an error correction code memory.

35. The method as claimed in claim 31, wherein executing the second startup initialization task comprises initializing a peripheral bus and associated devices.

36. The system as claimed in claim 25, wherein executing the first startup initialization task comprises initializing a peripheral component interconnect bus and associated devices.

37. A computer readable medium comprising first instructions associated with a first hardware initialization task and second instructions associated with a second hardware initialization task which, in response to being executed by a processor, result in the processor

executing the first hardware initialization task; and

executing at least a portion of the second hardware initialization during the first hardware initialization task.

38. The computer readable medium as claimed in claim 37, wherein the first instructions and the second instructions, in response to being executed by the processor, further result in

a first logical processor of the processor executing the first hardware initialization task, and

a second logical processor of the processor executing the second hardware initialization task.

39. The computer readable medium as claimed in claim 38, wherein the first instructions, in response to being executed, further result in the first logical processor initializing an error correction code memory.

40. The computer readable medium as claimed in claim 39, wherein the second instructions, in response to being executed, further result in the second logical processor initializing a peripheral component interconnect bus and associated devices.